

# M81016P/FP/KP

OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

## DESCRIPTION

M81016 is octal D-type flip-flop driver by 20-pin package. It has 8 same circuit units which is composed of D-type flip-flop logic circuit and high voltage NchMOS output transistor. M81016 has a common direct clear input and a common clock input.

## FEATURES

- Lineup with three packages
- High breakdown voltage ( $BV_{DSX} \geq 40V$ )
- Drain output current ( $I_{DS(max)} = 200mA$ )
- With input protection diodes
- Pin assignment of input-output flow through
- Wide operating temperature range ( $T_a = -40$  to  $+85^\circ C$ )

## APPLICATION

LED drive

## FUNCTION

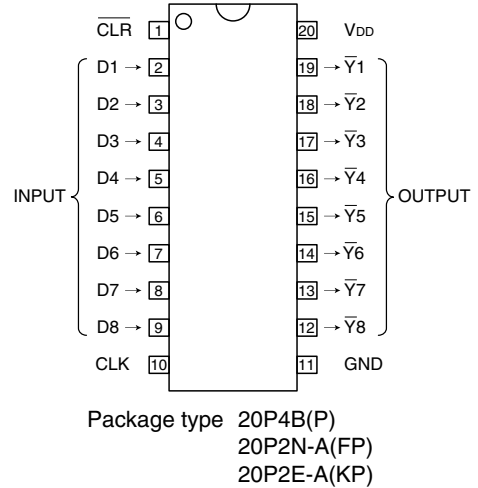
The common direct clear input and common clock input are connected to every circuit unit by the same way. Signal at the D inputs is transferred to  $\bar{Y}$  outputs by D-type flip-flops on the positive-going edge of the clock pulse.

If  $\overline{CLR}$  is set to "L", outputs  $\bar{Y}1$ - $\bar{Y}8$  will be altogether set to "H" regardless of D1-D8 and CLK.

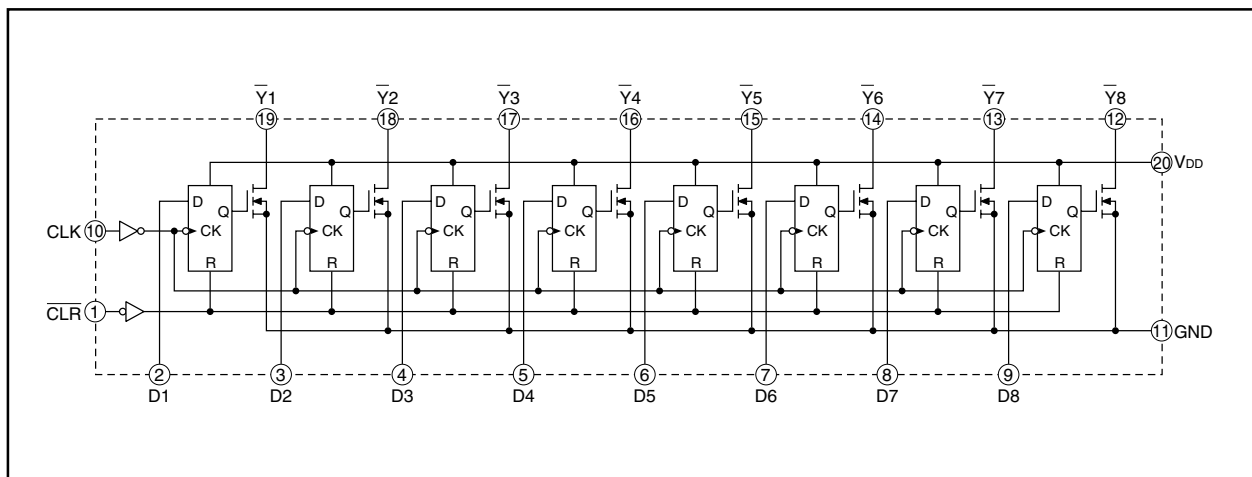
The maximum drain current of an output is 200mA. The maximum between drain-source is 40V.

Moreover, M81016FP/KP can save space with mini-flat package.

## PIN CONFIGURATION (TOP VIEW)



## LOGIC DIAGRAM (POSITIVE LOGIC)



# M81016P/FP/KP

## OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

### FUNCTION TABLE (EACH CHANNEL)

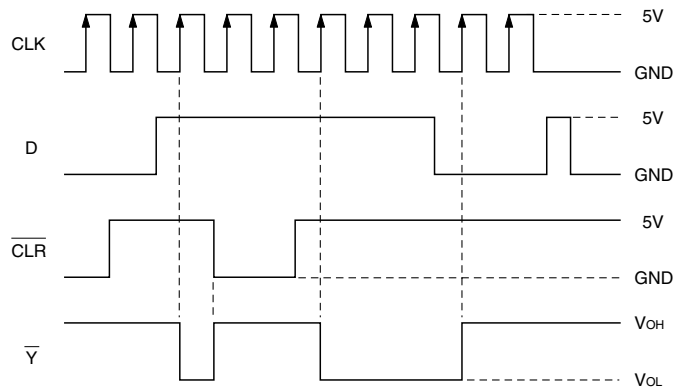
INPUT			OUTPUT : $\bar{Y}$
$\overline{\text{CLR}}$	CLK	D	
L	X	X	H
H	↑	L	H
H	↑	H	L
H	L	X	Latched
H	↓	X	Latched

H : High level

L : Low level

X : Irrelevant

### TIMING DIAGRAM



### ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, Ta = -40 ~ +85°C)

Symbol	Parameter	Conditions	Ratings	Unit	
V <sub>DD</sub>	Supply voltage		7	V	
V <sub>DS</sub>	Drain-to-source voltage	Output, H	-0.5 ~ +40	V	
V <sub>I</sub>	Input voltage		-0.5 ~ V <sub>DD</sub>	V	
I <sub>DS</sub>	Drain output current	Current per circuit output, L	200	mA	
P <sub>d</sub>	Power dissipation	Ta = 25°C, when mounted on board	M81016P	1.47	W
			M81016FP	1.10	
			M81016KP	0.68	
T <sub>opr</sub>	Operating temperature		-40 ~ +85	°C	
T <sub>stg</sub>	Storage temperature		-55 ~ +125	°C	

### RECOMMENDED OPERATING CONDITIONS (Unless otherwise noted, Ta = -40 ~ +85°C)

Symbol	Parameter	Conditions	Limits			Unit	
			min	typ	max		
V <sub>DD</sub>	Supply voltage		4.5	5.0	5.5	V	
V <sub>DS</sub>	Drain-to-source voltage		0	—	40	V	
V <sub>IH</sub>	"H" input voltage		0.7V <sub>DD</sub>	—	V <sub>DD</sub>	V	
V <sub>IL</sub>	"L" input voltage		0	—	0.3V <sub>DD</sub>	V	
I <sub>DS</sub>	Drain output current (Current per 1 circuit when 8 circuits are coming on simultaneously)	P	Duty Cycle no more than 45%	0	—	200	mA
			Duty Cycle no more than 100%	0	—	135	
		FP	Duty Cycle no more than 34%	0	—	200	
			Duty Cycle no more than 100%	0	—	120	
		KP	Duty Cycle no more than 18%	0	—	200	
			Duty Cycle no more than 100%	0	—	95	
V <sub>IN</sub>	Input voltage		0	—	V <sub>DD</sub>	V	
t <sub>r</sub> , t <sub>f</sub>	Rise time, Fall time, drain output	V <sub>DD</sub> = 4.5V	0	—	500	ns	
t <sub>su</sub>	Setup time before CLK ↑	V <sub>DD</sub> = 4.5V	20	—	—	ns	
t <sub>h</sub>	Hold time, data after CLK ↑	V <sub>DD</sub> = 4.5V	5	—	—	ns	
t <sub>w</sub>	Pulse duration	V <sub>DD</sub> = 4.5V	40	—	—	ns	
f	Clock frequency	V <sub>DD</sub> = 4.5V	—	—	20	MHz	

**M81016P/FP/KP**

OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted,  $V_{DD} = 5V$ ,  $T_a = 25^\circ C$ )

Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
$V_{(BR)DSX}$	Drain-source breakdown voltage	$I_{DS} = 1mA$	40	—	—	V
$I_{DSX}$	Drain-source leakage current	$V_{DS} = 40V$	—	0.002	5	$\mu A$
$I_{IH}$	"H" input current	$V_{DD} = 5.5V, V_i = 5.5V$	—	0.005	1	$\mu A$
$I_{IL}$	"L" input current	$V_{DD} = 5.5V, V_i = 0V$	—	0.005	-1	$\mu A$
$I_{CC}$	Supply current	$V_{DD} = 5.5V$	—	0.005	5	$\mu A$
		$V_i = 5.5V$ or $0V$				
$V_{DS}$	"L" output voltage	$I_{DS} = 100mA, V_{DD} = 4.5V$	—	0.25	0.38	V
		$I_{DS} = 200mA, V_{DD} = 4.5V$	—	0.51	0.77	
$R_{DS(on)}$	Drain-source on-state resistance	$I_{DS} = 100mA, V_{DD} = 4.5V$	—	2.5	3.8	$\Omega$

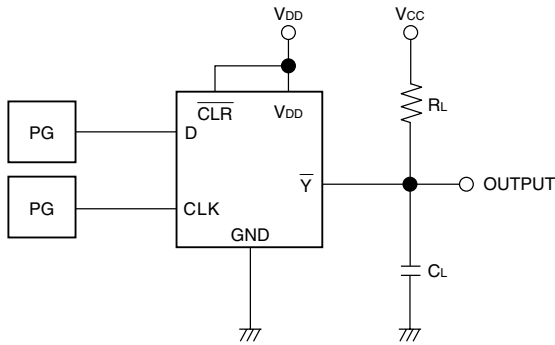
**SWITCHING CHARACTERISTICS** ( $V_{DD} = 5V$ ,  $T_a = 25^\circ C$ )

Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
$t_{TLH}$	Low-level to high-level and high-level to low-level output transition time	$C_L = 30pF$ (Note 1)	—	10	—	ns
$t_{THL}$			—	3	—	ns
$t_{PLH}$	Low-level to high-level and high-level to low-level output propagation time (CLK)		—	35	—	ns
$t_{PHL}$			—	30	—	ns
$t_{PLH(R)}$	Low-level to high-level output propagation time (CLR)		—	35	—	ns

# M81016P/FP/KP

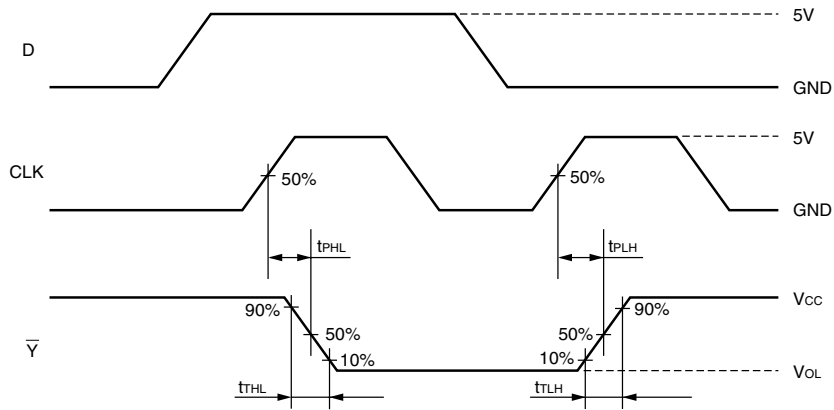
## OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

### NOTE 1 TEST CIRCUIT

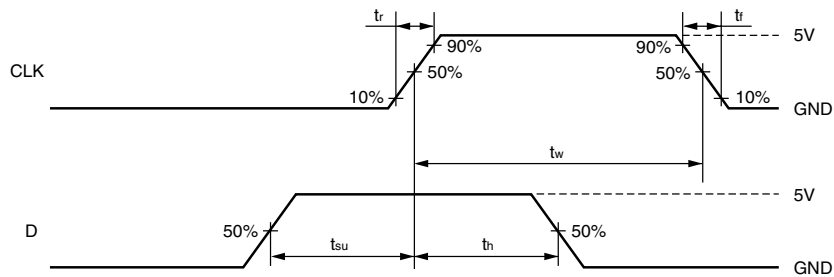


- (1) Pulse generator (PG) characteristics : PRR = 1MHz, Duty Cycle = 50%,  $t_r = 6ns$ ,  $t_f = 6ns$ ,  $Z_o = 50\Omega$ ,  $V_i = 5V$
- (2) Output conditions :  $R_L = 240\Omega$ ,  $V_{CC} = 24V$ ,  $V_{DD} = 5V$
- (3) Electrostatic capacity  $C_L$  includes floating capacitance at connections and input capacitance at probes.

### TIMING DIAGRAM



SWITCHING TIMES

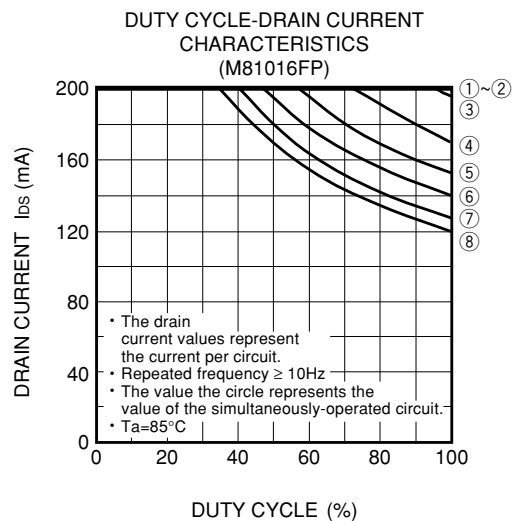
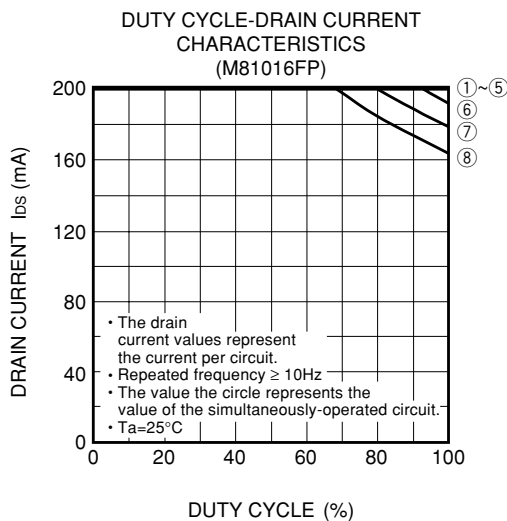
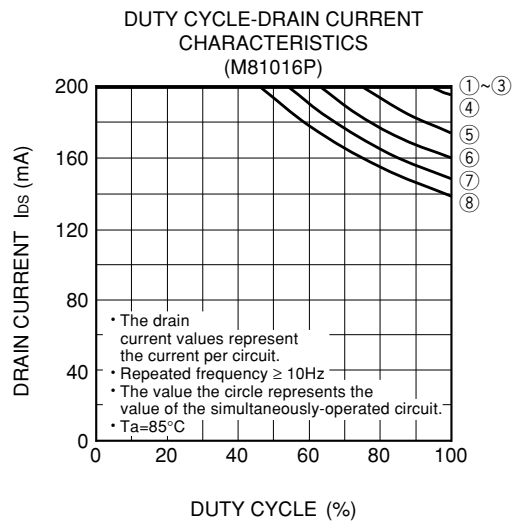
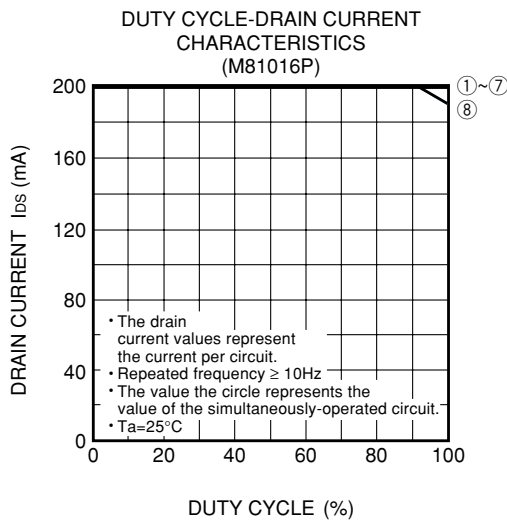
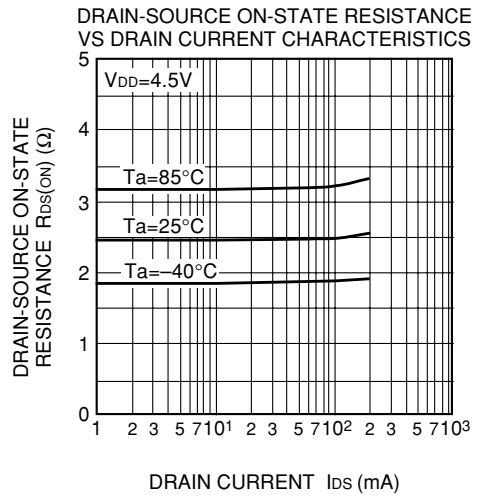
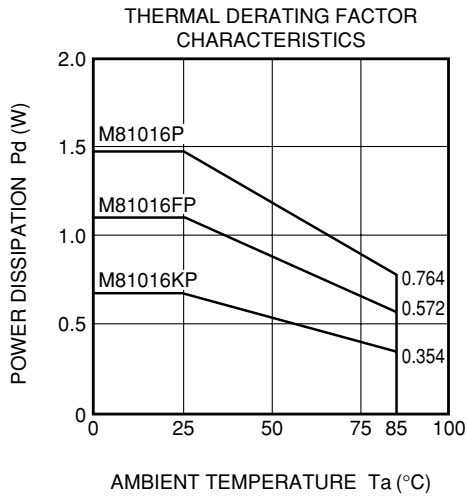


INPUT SETUP AND HOLD WAVEFORMS

# M81016P/FP/KP

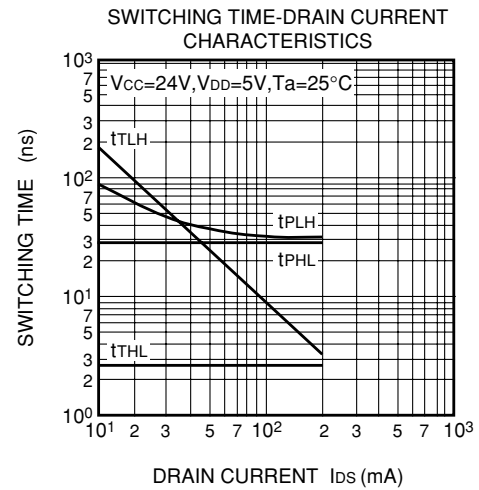
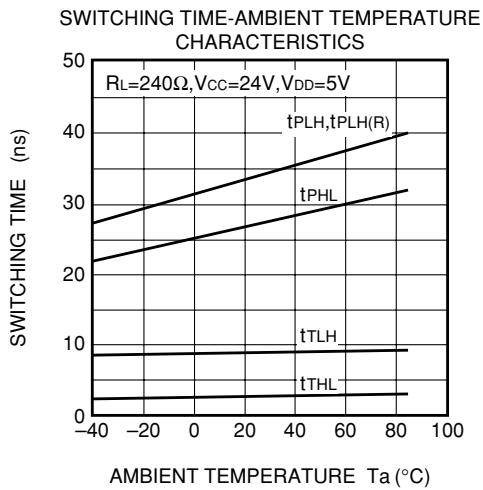
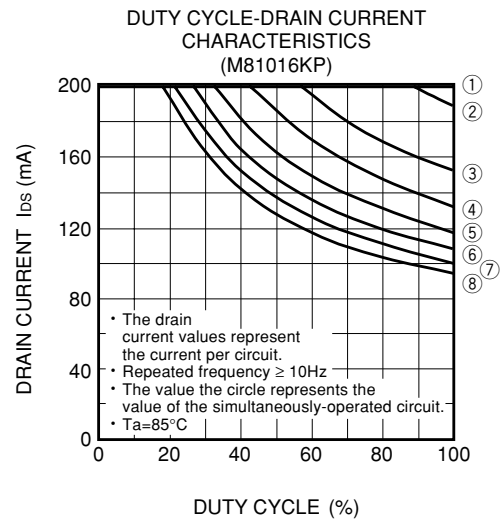
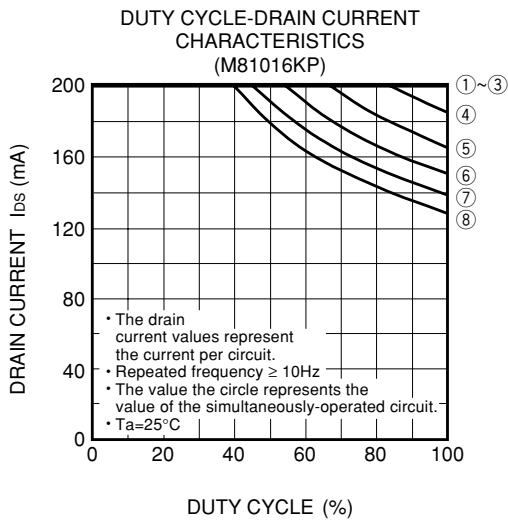
## OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

### TYPICAL CHARACTERISTICS



**M81016P/FP/KP**

OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

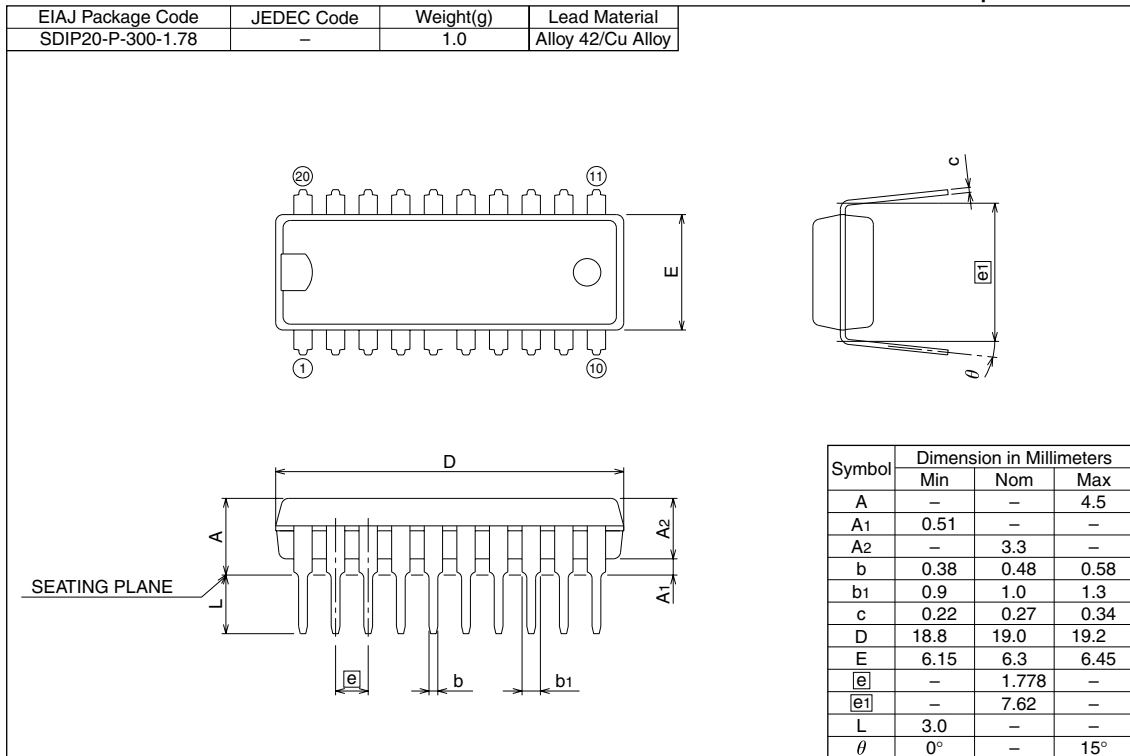


**M81016P/FP/KP**

OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

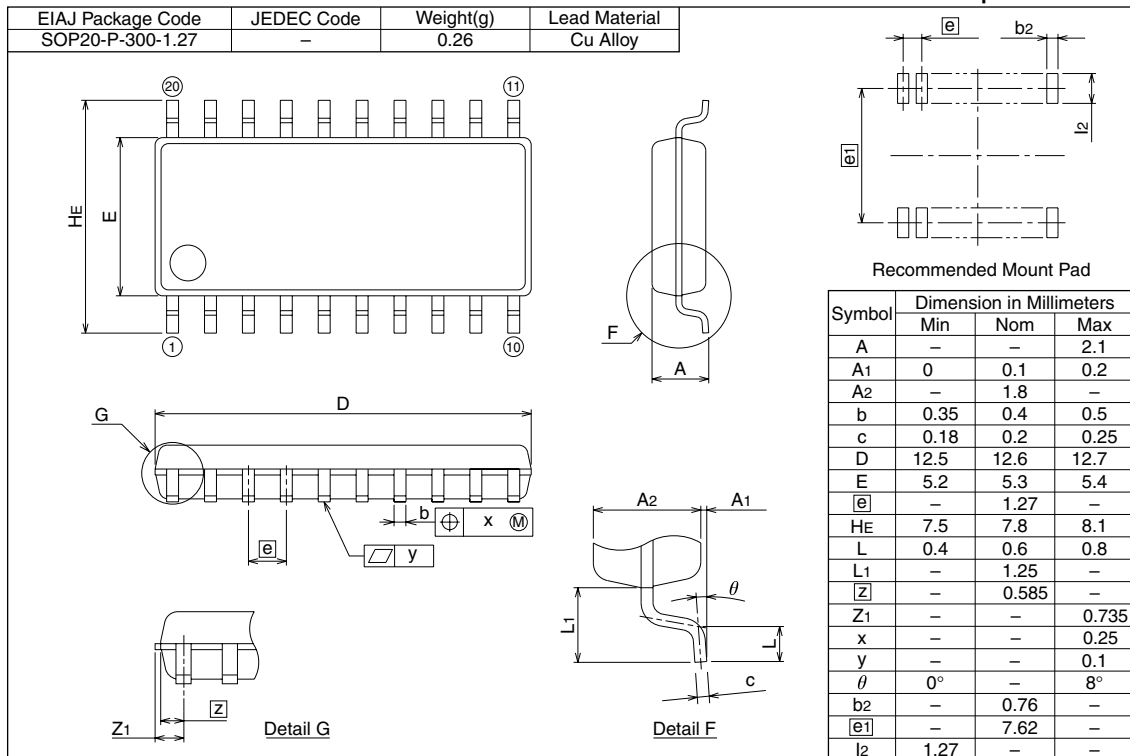
**20P4B**

Plastic 20pin 300mil SDIP



**20P2N-A**

Plastic 20pin 300mil SOP



**M81016P/FP/KP**

OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

**20P2E-A**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP20-P-225-0.65	-	0.08	Alloy 42

**Plastic 20pin 225mil SSOP**

